

S/N 09/751,610

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: William A. Harris
Serial No.: 09/751,610
Filed: December 29, 2000
Title: PRECISION PHASE GENERATOR

Examiner: Cassandra F. Cos
Group Art Unit: 2816
Docket: H16-26054 (256.058US1)

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SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicant respectfully requests that this Supplemental Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicant requests that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicant with the next official communication.

Pursuant to 37 C.F.R. §1.97(c)(1) and 37 C.F.R. §1.97(e)(1), Applicant state that each item of information contained in the Supplemental Information Disclosure Statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the Supplemental Information Disclosure Statement. Specifically, Applicant includes a copy of the International Search Report mailed on December 20, 2002 in PCT Application PCT/US 01/48976.

It is believed that no fee or statement is required with the Supplemental Information Disclosure Statement. However, if a final action under §1.113, a notice of allowance under §1.311, or an action that otherwise closes prosecution in the application has been mailed, the Commissioner is hereby authorized to charge the required fees to Account No. 19-0743 in order to have this Supplemental Information Disclosure Statement considered.

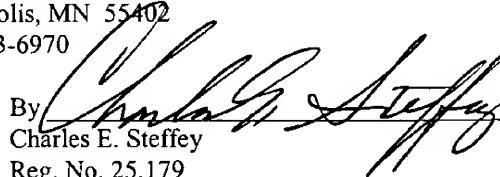
The Examiner is invited to contact the Applicant's Representative at the below-listed telephone number if there are any questions regarding this communication.

Respectfully submitted,

WILLIAM A. HARRIS

By his Representatives,

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By 
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Reg. No. 25,179

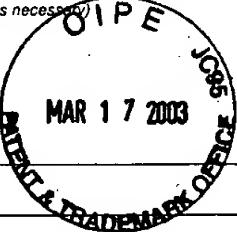
Date March 7, 2003

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 10th day of March, 2003

Gulim Abilova
Name

Gulim Abilova
Signature

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Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>		<i>Complete if Known</i>	
		Application Number	09/751,610
		Filing Date	December 29, 2000
		First Named Inventor	Harris, William
		Group Art Unit	2816
		Examiner Name	Cassandra F. Cox
Sheet 1 of 1		Attorney Docket No: H16-26054 (256.058US1)	

US PATENT DOCUMENTS

Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	Filing Date If Appropriate
	US-4,282,493	08/04/1981	Moreau, D. L.	331	2	07/02/1979

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	T ²
	DE-4214612	04/11/1993	Suwald, T.	H03K	23/40	
	EP-0526227	02/03/1993	Fujii, T.	H03L	7/87	

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		HAQUE, S. E., et al., "Phase-Locked Loop Based Linearly Controlled Three-Phase Firing Circuit for an AC Controller", <u>Int. J. Electronics</u> , 58, (1985), 761-767	
		SPARKES, R., et al., "Evaluation of Macro Models for Mixed Analog/Digital Circuits", <u>Proceedings of the IEEE 1998 Custom Integrated Circuits Conference</u> , Rochester, NY, (05 16 1988), 3.4.1 - 3.4.6	

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EXAMINER

DATE CONSIDERED